Reliability Report

BE Qualification

Transfer From NFME to CARSEM

UAT3 - LD39020DTPU13R

VFDFPN 1.0X1.0X0.38 4L PITCH 0,6

General Information	
Product Line	UAT301
Product Line Desc	200 mA very low quiescent current linear regulator IC
P/N	LD39020DTPU13R
Product Group	AMS
Product division	General Purpose Analog & RF Division POWER MANAGEMENT
Package	VFDFPN 1.0X1.0X0.38 4L PITCH 0,6
Silicon Process technology	BCD8sp

Locations	
Wafer fab	CTM8
Assembly plant	CARSEM China
Reliability Lab	CATANIA
Reliability assessment	PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	March 2018	9	Giuseppe Failla	Giovanni PRESTI	Preliminary Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
PCB	Printed Circuit Board

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Change BE (Subcontractor): The product family (LD39020XX) assembled in VFDFPN 1.0X1.0X0.38 4L PITCH 0.6 , will be transferred from NFME to CARSEM CHINA

Generic Data Available

- Many other Products assembled in CARSEM China (FPN package) - with dice diffused in BCD8 are already qualified.
- On the product under qualification (LD39020), the **DOE** has been completed in CARSEM with Positive results.

Starting from the above considerations, one assembly Lot is requested for the Reliability Verification

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that the *preliminary* reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

The reliability verification is running

4 DEVICE CHARACTERISTICS

4.1 Device description

LD39020

200 mA very low quiescent current linear regulator IC

Datasheet - production data

DFN4 1x1

SOT23-5L

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low dropout voltage (200 mV typ. at 200 mA load)
- Very low quiescent current (20 µA typ. at no load, 0.03 µA typ in off mode)
- Output voltage tolerance: ±0.5% (A version) or ± 2.0% @ 25 °C (standard version)
- 200 mA guaranteed output current
- High PSRR (80 dB@1 kHz, 50 db@100 kHz)
- Wide range of output voltages available on request: from 0.8 V up to 5.0 V in 50 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Optional output voltage discharge feature
- Compatible with ceramic capacitor C_{OUT} = 0.47 µF
- Internal constant current and thermal protections
- Available in DFN4 1x1 and SOT23-5L
- Operating temperature range: -40 °C to 125 °C

Applications

- Mobile phones
- Personal digital assistants (PDAs)
- Digital still cameras (DSC)
- Cordless phones and similar battery-powered systems
- Portable media players

Description

The LD39020 high accuracy voltage regulator provides 200 mA of maximum current from an input voltage ranging from 1.5 V to 5.5 V, with a typical dropout voltage of 200 mV.

It is available in DFN4 1x1 and SOT23-5L packages, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra low drop voltage, low quiescent current and low noise features, together with the internal soft-start circuit, make the LD39020 suitable for low power battery-operated applications.

An enable logic control function puts the LD39020 in shutdown mode allowing a total current consumption lower than 0.1 µA. Constant current and thermal protection are provided.

4.2 Construction note

PN	LD39020DTPU13R
Wafer/Die fab. information	
Wafer fab manufacturing location	CTM8
Technology	BCD8
Process family	BCD8sP
Die finishing back side	RAW SILICON
Die size	511, 511 micron
Bond pad met. Layers	Ti/AlCu/TxTN
Passivation type	TEOS/NITRIDE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ASL1000
Test program	SUAT3_0100.nx4
Assembly information	
Assembly site	CARSEM China
Package description	VFDFPN 1.0X1.0X0.38 4L PITCH 0.6
Molding compound	EPOXY
Frame material	-NIPDAUAG
Die attach material	EPOXY
Wires bonding materials/diameters	W0.8-27-AUCL-AL4-GLD-TNK
Final testing information	
Testing location	CARSEM China
Tester	ETS364
Test program	LD39020_13V_FT_10

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

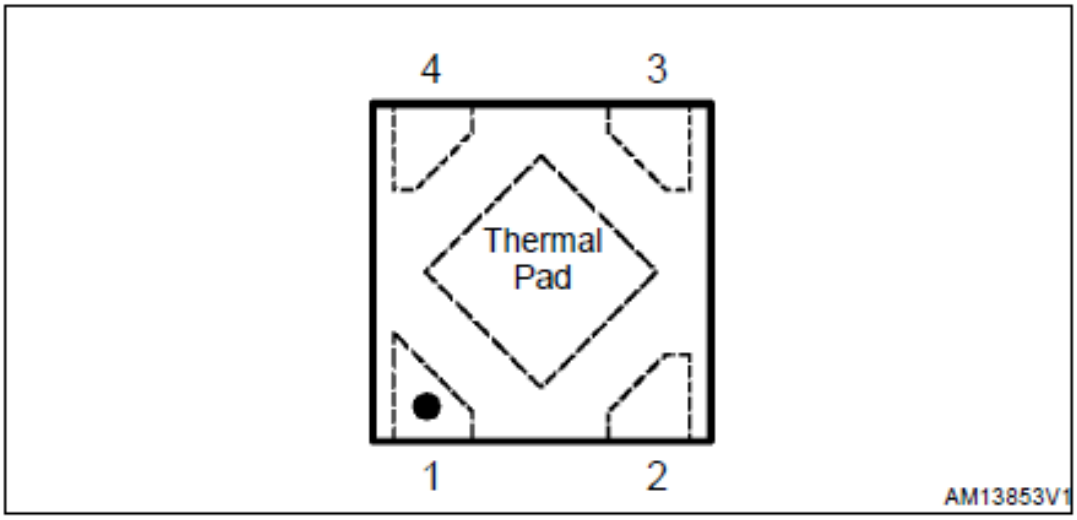
Lot #	Technical Code	Package	Product Line
1	1QBB*UAT3AB5	VFDFPN 1.0X1.0X0.38 4L PITCH 0.6	UAT301

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
Die Oriented Tests							
HTS	N	JESD22 A-103	Ta = 150° C		168 h 500 h 1000 h	0/45 run	
HTOL AMR, Low Power diss.	N	JESD22 A-108	Ta = 125° C, BIAS= +7 V		168 h 500 h 1000 h	0/77 run	
HTOL applicative	N	JESD22 A-108	Ta = 125° C, BIAS= +5.5 V		168 h 500 h 1000 h	0/77 run	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125° C Store 168 H @ Ta=85° C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		168 h	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121° C		96 h	0/77	
TC	Y	JESD22 A-104	Ta = -65° C to 150° C		100 cy 200 cy 500 cy	0/77 run	
THB	Y	JESD22 A-104	Ta = 85°C, RH = 85%, BIAS= +7 V		168 h 500 h 1000 h	0/77 run	
Additional Tests							
ESD		ANSI/ESDA/ JEDEC JS001-2014	CDM+/- 250V / 500V(All Pins)	3		pass	
CA			Construction Analysis			pass	

6 ANNEXES

6.1 Device details



Pin n°	Symbol	Function
1	OUT	Output voltage
2	GND	Common ground
3	EN	Enable pin logic input: Low = shutdown, High = active
4	IN	Input voltage
Thermal pad	GND	Connect to GND on the PCB

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Additional Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
CA Construction Analysis	Physical Analysis	To perform an internal and external analysis on devices, checking that the product is in line with ST specification.